C O N T E N T S

1. PERSONAL INFORMATION

Surname:	**Tassis**
Name:	**Dimitrios**
Name of Father:	**Hariton**
Year of birth:	1967
Place of Birth:	Thessaloniki
Marital status:	Married and father of four children
Address:	D.D. Lagynon
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2. DEGREES AQUIRED

BSc in Physics: Physics Department of the University of Ioannina, grade "very good", September 1990.

Master (M. Eng .): University of Leeds (Great Britain), Department of Electronic and Electrical Engineering, February 1993.

Ph. D.: Aristotle University of Thessaloniki, Physics Department, grade "excellent", January 2000.

3. ACADEMIC CAREER

January 2012 – Today: Assist. Professor at the Physics Department of the Aristotle University of Thessaloniki.

4. TEACHING EXPERIENCE

- Undergraduate courses:
  1. Introductory Physics Laboratory (2nd Semester)

2. Applied Informatics Laboratory (1st Semester)
3. Solid State Physics Laboratory (8th Semester)
4. Experimental Techniques for the study of Electrical Properties of Magnetic – Spectroscopic Materials (8th Semester)

- Postgraduate courses:
  1. MATERIALS CHARACTERIZATION TECHNIQUES: THEORY AND LABORATORY (Section: Electrical Characterization Laboratories), PPS: Materials Physics and Technology
  2. Training Workshops on Research Methodology - Simulation of Semiconductor Devices (with Silvaco-Atlas) (Project: Elective), PPS: Materials Physics and Technology
  3. Training Workshops on Research Methodology - Noise in semiconductor devices (Project: Elective), PC: Materials Physics and Technology
  4. TECHNOLOGY OF SEMICONDUCTOR DEVICES, PPS: Electronic Physics (Radioelectrology)

- I contributed to the writing of the textbook and the organization of the new course "Solid-State Physics Laboratory ", assuming the laboratories listed in "electrical measurements". The textbook will be issued shortly in a book that will be the main course textbook.

The evaluation of students, as delivered by the Quality Assurance Unit (MODIP) of the Aristotle University of Thessaloniki, through the Evaluation Committee of the Department, is available. A scan of the official document of this evaluation, as delivered to the Committee assigned to decide for my permanent tenure, is offered in the Annex (section 16). The rankings that I gathered is always much higher than the average for teachers in the same lesson, as well as from their respective averages of the Physics Department of the Aristotle University of Thessaloniki. An explanation of the meaning of the scores is given in the first scan, explaining that results in parenthesis refer to the average of the instructors in the same course, or the department's average.

Alongside my research work, in the years 1999-2012, I taught Physics and Technology in Secondary Education and specifically at the private school "The Apostle Paul". Also, I took over the teaching and evaluation in courses of Physics and Electronics in "G.C.E. Vakalis-Foundation" (preparing prospective students for studies in universities in Britain) in the sections of Engineers, during the school year

1995-96. Finally, I taught computer courses (Microsoft Windows, Word, Excel, Access and Programming) in the Hellenic Physical Society during the school years 1998-99 and 1999-2000.
During the period 2010-12, I was tutor in the "Major Program of Education (MPE)" of the Ministry of Education, after open call and certain qualification criteria being set. After successful certification in new teaching methods in Sciences, I trained Secondary School teachers, specialty PE4 (Physicists, Chemists, Biologists, Geologists), through a 200-hour seminar.

5. COMMITTEES

Member of the following committees of the Department:

1. COMMITTEE OF ORGANIZATION REPORTING, DATA COLLECTION, ACTIVITY & EDUCATIONAL CAPACITY, which is responsible for data collection and reporting the Department's evaluation (Internal Evaluation Group).

2. STUDIES ADVISOR COMMITTEE, AND STUDENT'S RECEPTION, that is responsible for the reception of freshmen. Members of the Committee, take on as mentors for students until they graduate.

3. ERASMUS-ECTS/DS COMMITTEE.

4. LINKING WITH SECONDARY EDUCATION COMMITTEE, because of my experience in the Secondary Education.

I have been responsible – representative of the Department of Physics (of the A.U.Th.) for the program **ERASMUS-MUNDUS**, referred to the Department's cooperation with foreign Universities, in order to exchange students and staff (except for countries covered by the ERASMUS+).

I was responsible – representative of the Department of Physics (of the A.U.Th.) for the program **ERASMUS+ International.**

Responsible – Coordinator of the Department of Physics for the acquisition of ECTS label.

I am **(elected) Member** of the General Assembly and the General Assembly of Special Composition in the Department of Physics of the Aristotle University of Thessaloniki.

I participated in the last **reformation-modernization of the curriculum of the Master's Degree Program of Postgraduate Studies (PPS)** "Electronic Physics (Radioelectrology)", of the Department of Physics, that took place in the year 2016. This master course is the 3rd oldest in Greece with a long tradition. Recently it celebrated its 50 years of operation.

6. ORGANIZING CONFERENCE COMMITTEES

Member of **the Organizing Committee** of the "**XXXI Panhellenic Conference on Solid State Physics & Materials Science**", held in Thessaloniki on 20-23 September 2015.
Member of **the Organizing Committee** of the "**11th European Conference on Silicon Carbide and Related Materials (ECSCRM)"**, held in Halkidiki on 25 – 29 September 2016.
Member of the **Scientific Committee of the "International Conference on Modern Circuits and Systems Technologies (MOCAST)"** during the years 2015 & 2016 & 2017, held in Thessaloniki.
Member of **Scientific Committee** of "**17th World Textile Conference AUTEX 2017**" that will be held in Corfu on 29-31 May 2017.

7. SUPERVISION OF THESES

7.1 Doctoral theses (main supervisor)

1. Stefanakis Dionysius, "**Development of nanoscale vertical field effect transistor of silicon carbide (SiC)**", in progress since January 2014.
2. Loyris Evangelos "**Construction and optimization of organic wearable electronics and circuits on substrates of fabrics with different structures"**, in progress since June 2016.

7.2 PhD thesis (an academic Advisory Committee member)

1. Fasarakis N., "**Nano-scale Multi-Gate MOSFETs: Compact models for the Drain Current and Noise for Development of Automated Design Tools of Nano-Electronics**", December 2014.
2. Karatsori T., "**Electrical Characterization and modelling of advanced nano-scale ultra thin body and buried oxide MOSFETs and application in circuit simulations** ". In stage of writing.

3. Messaris I., **“Modelling of nano-scale transistors for circuit simulation”**. "in progress.
4. Oproglidis T. **“Nanoscale triple gate MOSFET in SOI substrates: FinFET with orthogonal cross section without heterojunctions (Junctionless) and cylindrical FinFETs (nanowire-like)”**. In progress.
5. Kaimakamis T. In progress – setting the subject title (organic transistors).

7.3 Master Dissertations

1. Karatsori T., “**Analysis – prediction nanoscale FinFET transistor variability**", 2013.
2. Sidiropoulou P., '**Study of parasitic capacities in triple gate FinFET transistors without impurities or low concentration of impurities**", 2013.
3. Tsiara A., "**Simulation of nanoscale triple gate FinFETs, with TCAD tools-A comparative study**", 2015.
4. Oproglidis T., **“Optimization of multigate nano-transistors without heterojunctions (Junctionless FinFETs) and comparison with conventional FinFETs, by means of TCAD simulations”,** 2015.

Currently, **I am training-instructing four graduate** students (three from the PPS in “Electronic Physics” and one of the PPS in “Materials Physics and Technology”) to the simulation of nano-devices and parameter extraction of the transistors (based on our compact models but also with Silvaco Utmost) for applications in SPICE. We will soon define the title of their Master Theses.

7.4 Dissertations

1. Athanasiadis I., “**Study of FinFET transistors”**, 2013.
2. Daldaras E., “**Study of multi gate nano-transistors, with or without heterojunctions (conventional and junctionless FinFETs)”**, 2016.

8. PROFESSIONAL EXPERIENCE

Since October 1992 I work as a researcher in the Solid-State Physics section, in the **“Electrical Characterization & Design of Micro- and Nano-Electronics Devices laboratory” (MINED) of the Physics Department of the Aristotle University of Thessaloniki**. Until now I participated in **18 research projects,** with total working time of **more than 10 years** .

Besides the electrical characterization of materials and devices, I gained experience for characterizing semiconductor devices by developing automated measurement systems. These systems include apparatus for measuring: Hall, I-V, C-V, C-T, DLTS, Capacitance Transient Spectroscopy, phenomena of hot carriers with electrical stress, as well as noise measurements at low frequencies (LFN). Specifically, I developed applications in Bridgeview 2.1 environment (engine from LabView 5.1) and Labview 6, to control two measuring systems by computers in order to automate the experimental procedure. The first system, which includes computer, electrometer, two voltage sources, two spectrum analyzers, two current to voltage converter – with amplifier and NiCd batteries, is used for electrical characterization of diodes with current and electrical noise measurements. The second system has three voltage sources, one current source and pulse generator (preset and arbitrary - programmable), capacitance meter, programmable relais and oscilloscope, all controlled via GPIB. This setup is capable to (electrically) stress the device under test (DUT) by applying of DC voltage or current or even pulses. In both systems is possible to control the temperature of the sample through a cryostat. All the above equipments are controlled by their respective computers which coordinate the instruments and record the measurements.

We used the G programming language (graphical programming language with modules), which enables the design of virtual instruments, through which "real ones" are controlled and experimental facilities, through GPIB and VISA Protocols. At the same time, there is the possibility of processing of the measurements in real time, in order to directly evaluate important parameters characterizing the semiconductor devices. This is especially important in the case of "device stressing" in order to know the "damage" of the device while it is still under test.

More recently, in the laboratory equipments, a semiconductor characterization system: Keithley 4200SCS was added. This system uses the environment KITE (The Keithley Interactive Test Environment), which is based on the LabView programming environment, so there is the possibility to intervene and modify the software, in order to improve its measurements techniques or even adding new ones. This unit has four independent "Source Measure Unit" (SMU) and two Multi-frequency capacitance /voltage unit (CVU), that can measure both the very low currents, and capacitances (appearing in modern nano-devices).

I have worked on the following mainframe computers: CYBER, VAX, AMDAHL, workstations: Silicon Graphics, Sun, HP and of course PC compatibles. I know the Unix operating systems (and X Windows, OpenWin), DOS and MS-Windows. I was taught the design program AUTOCAD, as well as programs SATCAM, ORCAD and SPICE.

I program in the following programming languages: Basic, C, Fortran, Mathcad, Mathematica and Matlab, as well as in LabView environment (G language). I am especially interested in numerical methods for the analysis of experimental data and development-implementation of theoretical models for the simulation of semiconductor devices. The implementation and testing of theoretical models is done either with the help of conventional programming languages, or with commercial simulation programs (**Silvaco: Atlas, Devedit, Athena and Synopsys: Sentaurus**), where programming is also required. These programs theoretically have the ability to simulate the electrical behavior of any semiconducting device or material. Building the device can even start from the growth stage. We used these programs not only to successfully interpret and analyze the operation of multi gate nano-transistors **(double-gate,tri-gate,gate all around, nanowire transistors**), but also to investigate the importance of manufacturing parameters, thus optimizing the electrical characteristics of the devices.

Also, combining simulation programs with experimental measurements, we can examine the validity of the simulations (also adjusting the individual model parameters), thus reproduce the experimental data and then design (and evaluate) devices that still have not been manufactured yet. In this way we are able to change any parameter of the device under study and "produce" complete sets of samples that help us to evolve our theoretical models for the description of currents and capacitances of modern semiconductor nano-devices.

9. RESEARCH PROJECTS

Participation in the following research projects:

- «***Μελέτη της αδρανοποίησης βαθέων παγίδων στον ημιαγωγό GaAs με τη μέθοδο της ανόπτησης σε ατμόσφαιρα πλάσματος υδρογόνου***», **ΠΕΝΕΔ91, 1993-1995.** Coordinator: *Eleni Paloura*.
- ***«Το υποξείδιο του χαλκού (Cu_2O) σαν βασικό υλικό παρασκευής φωτοβολταϊκών στοιχείων και υπεραγωγών υψηλών θερμοκρασιών»*, ΠΕΝΕΔ91, 1993-1995.** Coordinator: *Leonidas Papadimitriou*.
- «***Υλικά με βάση το πυρίτιο για οπτοηλεκτρονικές διατάξεις»*, ΠΕΝΕΔ95, 1996-1998.** Coordinator: *Charalampos Dimitriadis*.
- **"*Procedures for the early phase evaluation of reliability of electronic components by development of CECC rules (PROPHESY)*", Contract No**

SMT4-CT95 2020, 1996-1997, (Sub-contractor Ε.Κ.Ε.Φ.Ε. "Δημόκριτος", Ινστιτούτο Μικροηλεκτρονικής), Coordinator: *Χαράλαμπος Δημητριάδης*.

- «***Ανάπτυξη της τεχνολογίας λεπτών υμενίων του TiN σε υποστρώματα Si για εφαρμογές σε διάφορες ηλεκτρονικές διατάξεις***», **ΠΕΝΕΔ95, 1996-1998.** Coordinator: *Charalampos Dimitriadis*.
- "***Development of diamond type thin film technology for electronic devices and flat panel display applications",* ΠΕΝΕΔ99, 1999-2000.** Coordinator: *Charalampos Dimitriadis*.
- "***Prossesing of low cost materials for microelectronics",* 1999-2002. ΕΠΕΤ ΙΙ, ΓΓΕΤ, «Μετάκληση Ελλήνων του Εξωτερικού».** Coordinator: *Theodoros Karakostas*.
- ***"Study and model development of TFT transistors - Design of TFT circuits and ion Li batteries for their supply",* ΠΥΘΑΓΟΡΑΣ, Υπουργείο Παιδείας, 2004-2006.** Coordinator: *Charalampos Dimitriadis*.
- "***Study of particle irradiation-induced defects in SiC rectifying contacts***", **Διμερής επιστημονική συνεργασία Ελλάδας-Πολωνίας, 2004-2005.** Coordinator: *Charalampos Dimitriadis*.
- "***Growth and characterization of semiconducting Silicide β-$FeSi_2$ Nanocrystals on Silicon***", **Διμερής επιστημονική συνεργασία Ελλάδας-Ουγγαρίας, 2004-2005.** Coordinator: *Charalampos Dimitriadis*.
- **"Study of ballistic nanotransistor MOFSET and thin film transistor of microcrystalline silicon of industrial production". ΠΕΝΕΔ2003, 1/7/2004-31/12/2008.** Coordinator: *Charalampos Dimitriadis*.
- ***"Fabrication and investigation of Li-ion microbatteries for applications in microelectronics",* ΠΥΘΑΓΟΡΑΣ ΙΙ, 1/4/2005-31/12/2007.** Coordinator: *Leonidas Papadimitriou*.
- «***Βελτιστοποίηση της απόδοσης και αξιοπιστία φωτοανιχνευτών μακρού υπερύθρου κβαντικών σημείων InGaAs στο GaAs***», **Διακρατική συνεργασία με χώρες εκτός Ευρώπης (Ελλάδας-Κορέας). 1/12/2006 – 31/3/2008. project code 05-NON-EU-174.** Coordinator: *Charalampos Dimitriadis*.
- **"Nano-transistor multigate MOSFETs :Drain current and noise compact models - Development of electronic design automated design tools for nanoelectronics", Συνεργασία 2009. 7/6/2012 – 30/11/2012. Κωδικός έργου 09ΣΥΝ-42-998.** Coordinator: *Charalampos Dimitriadis*.

- **“Continuous Transistor Sizing Toolset for nanoscale IC optimization”, Συνεργασία 2011, 17/10/2013 – 31/12/2014.** Coordinator: *Nikolaidis Spyridon*.
- **“Compact modelling of emerging NANO-scale multi-gate MOSFETs and reliability simulation tool for robust analog & mixed signal design facilitation”, ARISTEIA II, 2014 – 2015.** Coordinator: *Charalampos Dimitriadis*.
- **«3-D Junctionless Si-Nanowire Memory Devices», ARISTEIA II, 2014-2015.** Coordinator: *Pascal Normand*.
- **“Optimization of Bridged-Grain (BG) Double-gate (DG) polycrystalline silicon thin film transistors (TFTs)”, ΕΛΚΕ, ΔΡΑΣΗ Β΄ Ενίσχυση Ερευνητικής Δραστηριότητας 2012, project code 89357.** Coordinator: *Dimitrios Tassis*.

10. SCIENTIFIC COMPANIES

Member of the Hellenic Physical Society (E.E.F.).
Member of the Scientific Society: Micro & Nano.

11. RESEARCH ACTIVITIES

11.1 Distribution of my research on thematic areas

a) Seniconducting Si

During my doctoral thesis I dealt with the semiconducting iron disilicide (b-$FeSi_2$), thus with semicunducting silicides, both in terms of growth (in the form of thin films), and the evaluation mainly of their electrical properties, such as conductivity, Hall-effect, magnetoresistance and electrical noise. The ultimate objective was the improvement of the material but also the successful use in electronic and optoelectronic devices. The β-$FeSi_2$ is of particular interest because of the direct energy gap it exhibits at about 0.85eV, making it an ideal material for the construction of optoelectronic devices working at wavelengths (of light) about at 1.5 mm (near infrared). With deposition of successive ultrathin layers of iron and Silicon in ultra-high vacuum (with solid phase epitaxy) and with appropriate annealing conditions (800 ^{o}C with rapid annealing for 30 s or 700 ^{o}C for 1 hour with conventional oven annealing), we managed to improve the mobility and the

concentration of the carriers by a factor of 100. Particularly interesting is the fact that, depending on the growing conditions, can occur either p, or n-type semiconductor.

Apart from the material, the heterojunctions b-$FeSi_2$ – Silicon (b-$FeSi_2$/Si) were manufactured and studied. The ideality factor is 2, indicating that the current is due to the generation-recombination mechanism of at the interface traps. With the low-frequency electrical noise technique, which was first implemented in this material, we determined the concentration of interface traps and found that it decreases when the silicide is developed with the rapid annealing process. Finally, we studied the electrical properties of quantum dots of b-$FeSi_2$ in Silicon, developed by the technique of molecular beam epitaxis (MBE). These samples were manufactured in the research laboratory of the Russian Academy of Sciences. In this field refer the publications 5-9, 11, 12, 21 and 35 (as described in section 12).

b) Thin Film Transistors (TFTs)

Electrical characterization of TFTs: 1) Thin film polycrystalline silicon transistors developed by LPCVD (Low Pressure Chemical Vapor Deposition). The semiconductor devices that we studied were supplied by the General Electric Company (England). 2) Thin film polycrystalline silicon developed by the SPC technique (Solid Phase Crystallization) and annealed with Excimer Laser. The studied samples were manufactured by the SEIKO-EPSON company (Japan). 3) Nano-crystalline Silicon thin film transistors grown by PECVD technique (low- temperature plasma enhanced chemical vapor deposition). These samples were obtained from CEA-LETI (Grenoble-France).

New experimental techniques were developed for the determination of the parameters of the transistor and the interface traps on the edge of the crystallites. The result of these studies was to identify the technological parameters that affect the performance of the semiconductor devices, thus improving their performance. Theoretical models have been proposed in order to describe the input and output (polycrystalline Si) transistor characteristics. Also, the interface (gate oxide - polycrystalline silicon interface) and bulk traps (within the semiconductor) were estimated. These models have been used successfully to develop a SPICE model, in order to simulate integrated circuits of TFTs. In addition, using the technique of (electrical) Low Frequency Noise (LFN) we were able to evaluate the quality of gate oxide contact/polycrystalline film interface (by calculating the concentration of interface traps), as well as the quality of the channel (from the calculation of the concentration of the bulk traps). Finally, we studied the degradation mechanisms of the transistor and their characteristics, due to the occurrence of hot carriers. This was achieved by imposing electrical stress (stress), applying either DC or trapezoidal

voltage pulses to the transistor (dynamic stress), for up to 10 times^{5} s. Thus, the spatial extent of the damage to the channel and the increase of the traps in the oxide /polycrystalline film interface close to drain, was estimated, for transistors with different groth techniques and geometries. In this field refer the publications 1-4, 18, 19, 22, 23, 25-27, 32-34, 36-37, 39-41, 43-45, Σ3.

c) Quantum dots (QD's) of InAs in GaAs

The electrical properties of InAs quantum dot points in GaAs built with the technique of molecular beam epitaxis (MBE) were studied. Part of the samples were fabricated at IMEM Institute (Italy) and the rest in a laboratory of the Institute of Sciences and Technology of Korea. To identify the traps of the InAs within the energy gap of the GaAs, Shottky diodes Au/n-GaAs were built containing quantum dots of InAs. The electrical characterization was achieved by measuring the voltage-current measurements (I-V) characteristic, voltage-capacitance (C-V) dependence and the electrical noise at different temperatures. In this thematic area correspond the publications 20, 24, 28, 30, 32 and 42.

d) Semiconducting or metallic materials (a-C,TiN, SiC)

Amorphous carbon (a-C) thin films were studied, developed by dc reactive magnetron sputtering, in the LTFN laboratory (Department of physics, Aristotle University of Thessaloniki). Hall measurements indicated that the semiconductor is of p-type and the concentration of the holes is estimated. The electrical characterization was completed with measurements I-V (at different temperatures) and noise (at room temperature). The results were related to the growth conditions of the material. With proper growth conditions may be developed, except of a-C, nano-crystalline carbon (nc-C) can also be grown on silicon. So, heterojunctions a-C /Si as well as nc-C /Si were built. The electrical characterization was accomplished by measuring I-V, C-V and noise at different temperatures.

The metallic TiN shows very good electrical characteristics and is a promising material in semiconductor technology. The Shottky diodes of TiN/Si studied, were also manufactured in the LTFN laboratory, by dc reactive magnetron sputtering. The electrical characterization of the diodes (measured: I-V and electrical noise), determined the optimal conditions for the development of the material.

Silicon carbide is of great interest in power electronics applications, due to remarkable physical and electrical properties it exhibits. Though, it was not adequately studied yet, in order to reach the stage of industrial commercialization. Measurements of I-V, C-V and low-frequency electrical noise on contacts 4H-SiC p^{+}-

$n\text{-}n^+$ at room temperature were performed in order to determine the characteristics of interface and bulk traps.

In this thematic area correspond the publications 10, 13-17, 31.

e) SiC VJFET and power transistors

Silicon carbide is now a technologically mature solution and is almost perfect (compared to other semiconducting materials) for applications in power electronics. It is wide band gap semiconductor with high breakdown voltage –about ten times bigger than of silicon. Combining it with the VJFET geometry yields a potentially very good candidate for industry implementation with very competitive features. Thus, it is particularly interesting to study and optimize it.

Within this frame, we collaborate with the Foundation for research and Technology-Hellas (FORTH), where the transistor were produced, in order to evaluate and improve electrical characteristics of the devices. The measurements are used as feedback for the simulations on TCAD applications.

As a result of this cooperation, the co-supervision of a Ph.D. (Stefanakis D.) has occurred.

In this thematic corresponds S21, while more work is expecting to emerge, since the research has reached a critical point.

f) Organic and textile materials and transistor

Organic materials and transistors have some important advantages (lightweight, flexible, biodegradable, easy and economic construction, etc.). Although not reaching the performance of inorganic, they are very interesting for modern applications of technology. These materials find application also in smart textiles. The purpose of the research is for the transistor to shrink to the fiber level and form a complete circuit within the garment fabric – in contrary to what happens at the present by simply attaching circuits to the clothes.

Within this frame, we started the cooperation with the laboratory LTFN (Laboratory for Thin Films-Nanobiomaterials-& Nanosystems Nanometrology-Department of Physics, Aristotle University of Thessaloniki) -for organic transistors, and the Universities of Piraeus (Piraeus University of Applied Sciences, School of Engineering, Department of Textile Engineering) and Ghent (Ghent University, Faculty of Engineering and Architecture, Department of Textiles) - for organic and textile transistors.The cooperation is reinforced with two doctorates in co-supervision (Louris E. and Kaimakamis T).

In this thematic correspond S22 , S23 and S24.

(g) Multi gate nano-transistors (double-gate, triple-gate, FinFETs)

In a technology that requires constant shrinking of the size of the transistors, multi gate MOSFET transistors promise good operation even in the dimension of a few nanometers. The samples that we study, built by the IMEC (Belgium) and triple gate MOSFETs with gatelengths down to 20 nm. Using multiple gates has resulted in suppression of the short channel effects. For their study we use two-dimensional and three-dimensional simulation programs of Silvaco (Devedit and Atlas), as well as the corresponding TCAD program of Synopsys (Sentaurus). By comparing experimental data and simulations (and a feedback procedure) we were able to choose appropriate models (and adjust their corresponding parameter values) that describe the behavior of the transistors. Still, simulation tools are very important to the development of theoretical models for the electrical behavior of the transistor, since we can "construct" devices which to differ at will – in any construction detail, in order to check the validity of the model versus any parameter of the device. If the matching is not satisfactory, the simulated data will help to improve the model. Also, simulations help to control and improve the procedures for the estimation of the transistor parameters (parameter extraction)- we have developed- since we know in advance the "correct" values. If there is a discrepancy, the procedures have to be redesigned.

To automate the design of the devices, we use a series of programs -codes written in Matlab and Excel - which are combined with the tools of Silvaco in order to avoid possible errors that can occur with the direct use of the design program of Silvaco (Devedit) in a repeated manner. In this way also decreased dramatically the design time for each layout.

Making a comparative study of the behavior of transistors – with simulation-in a wide range of construction parameters, we can optimize the behavior of the device (device optimization), and make it compatible with the (future) demands requirements of the ITRS.

Also, by adjusting properly the devices for simulation, we can isolate effects on their behavior (such as: series resistors, parasitic capacities) in order to better interpret the experimental data (actual measurements).

The latest devices that we study are the (3D): **Junctionless FinFETs** (JL FinFETs), **Junctionless Nanowires** and (2D): **Full Depleted SOI** (FDSOI), causing the semiconductor industry's interest in further shrinking of the transistors and are the only remaining competitive in dimensions around 10 nm (gatelength). The most recent samples that we study were produced either in CEA-LETI (FDSOI and JL-FinFETs) or in the NATIONAL CENTER for RESEARCH in NATURAL SCIENCES "DIMOKRITOS" (JL-FinFETs), in ST Microelectronics (FDSOI), or at IMEC (FinFETs).

In this thematic area refer all the rest of my publications.

11.2 Recognition of my research contribution

I was reviewer for the following journals:

IEEE Transactions on Electron Devices
Nano
European Physical Journal - Applied Physics (EPJAP)
Solid State Electronics
Scientific Journal Facta Universitatis

The number of citations (excluding self-citations) that appear in the Science Citation Index until January 2017 is **795** (**h-index= 17**), as shown in section 15.

12. PUBLICATIONS

12.1 Academic theses

1. D.H. Tassis, "MUF and the Lorentz term", MSc Thesis, University of Leeds, Dept. of Electrical and Electronic Engineering, UK, October 1992.
2. D.H. Tassis, "Growth and characterization of the semiconducting silicide $FeSi_2$ and the $FeSi_2$/Si heterojunctions for optoelectronic applications", Aristotle University of Thessaloniki, Physics Dept., January 2000.

12.2 Articles in international Journals with referees

1. C.A. Dimitriadis, D.H. Tassis, and N.A. Economou, "Determination of bulk states and interface states distributions in polycrystalline silicon thin film transistors", J. Appl. Phys. **74**, 2919 (1993).
2. C.A. Dimitriadis, D.H. Tassis, N.A. Economou, and G. Giakoumakis, "Influence of deposition pressure on the bulk and interface states in low pressure chemical vapor deposited polycrystalline silicon thin-film transistors", Appl. Phys. Lett. **64**, 2709 (1994).
3. C.A. Dimitriadis and D.H. Tassis, "Output characteristics of short-channel polycrystalline silicon thin-film transistors", J. Appl. Phys. **77**, 2177 (1995).
4. C.A.Dimitriadis and D.H.Tassis, "On the threshold voltage and channel conductance of polycrystalline silicon thin-film transistors", J. Appl. Phys. **79**, 4431 (1996).

5. D.H. Tassis, C.L. Mitsas, T.T. Zorba, C.A. Dimitriadis, O. Valassiades, D.I. Siapkas, M. Angelakeris, P. Poulopoulos, N.K. Flevaris, and G. Kiriakidis, "Infrared spectroscopic and electronic transport properties of polycrystalline semiconducting $FeSi_2$", J. Appl. Phys. **80**, 962 (1996).
6. D.H. Tassis, C.L. Mitsas, T.T. Zorba, M. Angelakeris, C.A. Dimitriadis, O. Valassiades, D.I. Siapkas and G. Kiriakidis, "Optical and electrical characterization of high quality β-$FeSi_2$ thin films grown by solid phase epitaxy", Appl. Surf. Sci. **102**, 178 (1996).
7. D.H. Tassis, C.A. Dimitriadis, S. Boultadakis, J. Arvanitidis, S.Ves, S.Kokkou, S.Logothetidis, O.Valassiades, P.Poulopoulos and N.K.Flevaris, "Influence of conventional and rapid thermal annealing on the quality of polycrystalline β-$FeSi_2$ thin films grown from vapor-deposited Fe/Si multilayers", Thin Solid Films **310**, 115 (1997).
8. D.H. Tassis, C.A. Dimitriadis and O. Valassiades, "The Meyer-Neldel rule in the conductivity of polycrystalline semiconducting $FeSi_2$ films", J. Appl. Phys. **84**, 2960 (1998).
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12.3 Proceedings in International Conferences with referees

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Σ2. D.H.Tassis, C.L.Mitsas, T.T.Zorba, M.Angelakeris, C.A.Dimitriadis, O.Valasiades, D.I.Siapkas and G.Kiriakidis, "Optical and electrical characterization of high quality β-$FeSi_2$ thin films grown by solid phase epitaxy", Intern. Symposium on Si heterostructures: from physics to devices, 11-14 Sept. 1995, Heraklion, Crete, Greece.

Σ3. I.Pappas, A.T. Hatzopoulos, D.H. Tassis, N. Arpatzanis, S. Siskos, A.A. Hatzopoulos, C.A. Dimitriadis, and G. Kamarinos, "A Simple Polysilicon Thin-Film Transistor SPICE Model", Proc. 25th International Conference on Microelectronics (MIEL 2006) 480 (2006).

Σ4. A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, G. Pananakakis and G. Ghibaudo, "Transconductance to drain current ratio in nanoscale double-gate and cylindrical gate-all-around MOSFETs", 6th Intern. Conf. on Nanosciences & Nanotechnologies, July 13-15, 2009, Thessaloniki, Greece.

Σ5. A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, G. Ghibaudo, "Analytical threshold voltage model for asymmetrical dual-gate material short-channel double- gate MOSFETs", 4th International Conference on Micro- Nanoelectronics, Nanotechnologies and MEMs (Micro&Nano2010), December 12-15, 2010, Athens, Greece.

Σ6. I. Pappas, D. Tassis, s. Siskos and C. A. Dimitriadis, "Characteristics of Double-Gate Polycrystalline Silicon Thin-Film Transistors for AMOLED Pixel Design", Electronics, Circuits, and Systems (ICECS), 301 (2010).

Σ7. N. Fasarakis, A. Tsormpatzoglou, D. H. Tassis, I. Pappas, K. Papathanasiou, C. A. Dimitriadis, "Analytical Compact Modeling of Nanoscale Triple- Gate FinFETs", IEEE Mediterranean - Proceedings of the 16th Electrotechnical Conference (MELECON), 115 (2012) - IEEE Mediterranean, March 25-28, 2012, Medina Yasmine Hammamet, Tunisia.

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Σ9. N. Fasarakis, A. Tsormpatzoglou, D. H. Tassis, G. Ghibaudo, C. A. Dimitriadis, "Unified compact model of undoped or lightly doped short-channel cylindrical gate-all-around MOSFETs", 9th International Conference on Nanosciences & Nanotechnologies (NN12), July 3-6, 2012, Thessaloniki, Greece.

Σ10. N. Fasarakis, A. Tsormpatzoglou, D.H. Tassis, K. Papathanasiou, G. Ghibaudob, and C.A. Dimitriadis, "Compact modeling for undoped or lightly doped nanoscale trapezoidal and triangular FinFETs", 5th International Conference on Micro-Nanoelectronics, Nanotechnologies and MEMs (Micro&Nano2012), October 7-10, 2012, Heraklion, Greece.

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Σ12. P. Sidiropoulou, D.H. Tassis, N. Fasarakis, C.A. Dimitriadis, "Investigation of parasitic capacitances in undoped or lightly doped nanoscale triple-gate FinFETs", 10th International Conference on Nanosciences & Nanotechnologies (NN13), July 9-12, 2013, Thessaloniki, Greece.

Σ13. Tassis, D.H., Fasarakis, N., Dimitriadis, C.A., Ghibaudo, G. "Variability analysis-Prediction method for nanoscale triple gate FinFETs", 2013 IEEE International Semiconductor Conference Dresden - Grenoble: Technology, Design, Packaging, Simulation and Test (ISCDG 2013), Sep 26-27, 2013, Dresden, Germany.

Σ14. N. Fasarakis, D. H. Tassis, A. Tsormpatzoglou, K. Papathanasiou, C. A Dimitriadis, G. Ghibaudo. "Compact modeling of nano-scale trapezoidal cross-sectional FinFETs", 2013 IEEE International Semiconductor Conference Dresden - Grenoble: Technology, Design, Packaging, Simulation and Test (ISCDG 2013), Sep 26-27, 2013, Dresden, Germany.

Σ15. D. Tassis, "Optimization of Bridged-Grain polysilicon Thin-Film Transistor (BG-TFT)", 29th International Conference on Microelectronics (MIEL 2014), May 12-15, 2014, Belgrade, Serbia.

Σ16. D. Tassis, I. Messaris, N. Fasarakis, S. Nikolaidis, G. Ghibaudo and C. Dimitriadis, "Variability Analysis – Prediction Method for Nanoscale Triple Gate FinFETs", PROC. 29th INTERNATIONAL CONFERENCE ON MICROELECTRONICS (MIEL 2014), 99 (2014), May 12-15, 2014, Belgrade, Serbia.

Σ17. D.H. Tassis, T. Karatsori, A. Tsormpatzoglou, P. Dimitrakis, V. Ioannou-Sougleridis, P. Normand, C.A. Dimitriadis. "Optimization of junction and junctionless FinFETs", 38th WOCSDISE, June 15-18, 2014, Delphi, Greece.

Σ18. N. Fasarakis, C. G. Theodorou, A. Tsormpatzoglou, D. H. Tassis, G. Ghibaudo, C. A. Dimitriadis. "FinFETs: Compact modeling – low frequency noise", 38th WOCSDISE, June 15-18, 2014, Delphi, Greece.

Σ19. D. Tassis, I. Messaris, N. Fasarakis, A. Tsormpatzoglou, S. Nikolaidis and C. Dimitriadis,"Variability of nanoscale triple gate FinFETs Prediction and analysis method", 21th IEEE International Conference on Electronics, Circuits and Systems (ICECS), Article number 7050084, 710-713 (2015), December 7-10, 2014 Marseille, France.

Σ20. D.H. Tassis, T.A. Karatsori, C.G. Theodorou, G. Ghibaudo, and C.A. Dimitriadis, "Hot-carrier degradation of UTBB FD-SOI MOSFETS due to interface and silicon bulk traps", 6th International Conference on Micro- Nanoelectronics, Nanotechnologies and MEMs (Micro&Nano2015), 4-7 October 2015, Athens, Greece.

Σ21. K. Zekentes, K. Vassilevski, A. Stavrinidis, G. Konstantinidis, M. Kayambaki, K. Vamvoukakis, E. Vassakis, H. Peyre, N. Makris, M. Bucher, P. Schmid, D. Stefanakis and D. Tassis, "Modelling of 4H-SiC VJFETs with self-aligned contacts", Materials Science Forum, Vol. 858, pp. 913-916, (2016). Presented in 16th International Conference on Silicon Carbide and Related Materials, ICSCRM 2015, 4 - 9 October 2015, Sicily, Italy.

Σ22. E Louris, G Priniotakis, L Van Langenhove and D Tassis "From the Organic Thin Film Transistor to the 3-D Textile Organic Cylindrical Transistors – Perspectives, expectations and predictions", to be presented in 17th AUTEX, Corfu, 29-31 May 2017, Greece.

Σ23. E Louris, G Priniotakis, L Van Langenhove and D Tassis "Optimization of the Textile Organic Field Effect Transistors", to be presented in 17th AUTEX, Corfu, 29-31 May 2017, Greece.

Σ24. E Louris, G Priniotakis, L Van Langenhove and D Tassis "Optimizing the geometric characteristics of a fibre-based Textile Organic Field Effect Transistor using TCAD simulation tool", to be presented in 12th Joint International Conference CLOTECH 2017, Lodz, 11–14 October 2017, Poland.

12.4 Proceedings in Greek Conferences with referees

Σ25. A. Tsormpatzoglou, D. H. Tassis, C. A. Dimitriadis, M. Mouis, G Ghibaudo and N. Collaert, "Electrical Characterization and Design Optimization of Finfets with TiN/HfO_2 Gate Stack", 25th PanHellenic Conference on Solid State Physics & Materials Science, 20-23 Sept. 2009, Thessaloniki, Greece.

Σ26. A. Tsiara, D. Tassis and C. Dimitriadis, "Simulation of nanoscale triple gate FinFETs, with TCAD tools - A comparative study", 31st PanHellenic Conference on Solid State Physics & Materials Science, 20-23 Sept. 2015, Thessaloniki, Greece.

13. CONTRIBUTION IN CREATING RESEARCH INFRASTRUCTURE WITHIN A.U.Th.

I contributed actively in the development of automated layout research for **"Laboratory electric characterization of semiconductor materials and devices of microelectronics (MINED)"** of the Physics Department of the Aristotle University of Thessaloniki (http://mined.physics.auth.gr/).
My contribution has to do both with the connection of "real" instruments (wiring, grounding study, isolation from noises and interference), and software development – creation of "virtual instruments", as stated in more detail in Chapter 8 (professional experience). This experimental setup is updated frequently with new techniques, adding new instruments and by developing programs that allow them to communicate with the existing infrastructure.
I also, maintain and update the computer network of the lab that is dedicated exclusively to simulations. This network includes computers with MS-Windows and Linux (RedHat) operating systems, properly configured in order to "run" the simulation packages (TCAD) of Silvaco and Sentaurus.

Undergraduate-Graduate workshops

I am the coordinator and responsible for the laboratory infrastructure and organization of the "Laboratory of Electrical Characterization" of the PPS: Materials Physics and Technology, supporting courses such as "Materials characterization techniques and Laboratories".

I am the coordinator and responsible for the laboratory infrastructure and organization of the "Solid State Laboratory" (Electrical Characterization part) which supports

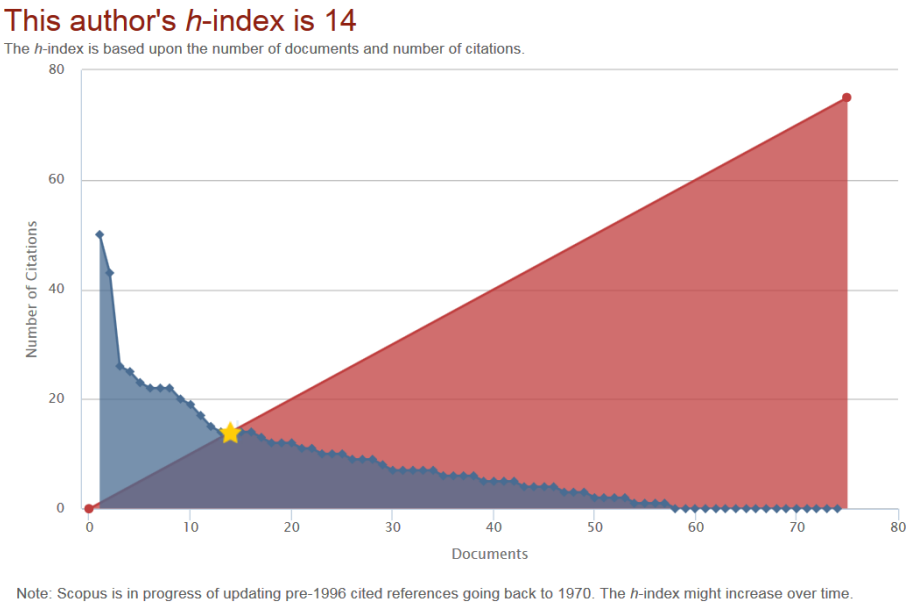
courses such as “Laboratory techniques for the study of electrical properties of Magnetic – Spectroscopic Materials”.

14. OTHER SCIENTIFIC WORK

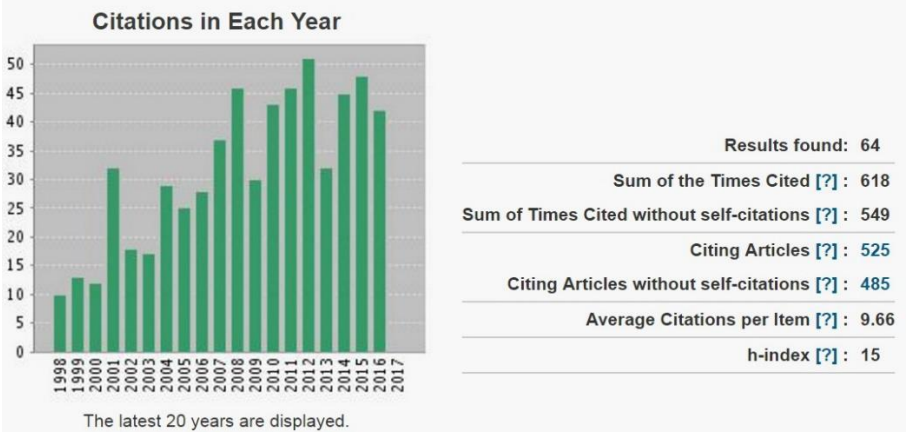
I had the responsibility and scientific supervision of translation – adjustment to the Greek reality, software that is used in the teaching of technology in Secondary Education (PRIME software: Design & Technology). Also assumed writing twenty accompanying laboratory exercises. The above is distributed in selected schools of Greece for the teaching of Technology, within the framework of the program funded by the Greek Ministry of Education: KIRKI.

15. REFERENCES ON MY PUBLICATIONS

In **Scopus** there are registered 702 total references, of which 612 are non self-citations (source: **www.scopus.com**, author search: Tassis D.H., Author ID: 6603597934), yielding an **h-index= 14**.



Similar are the results from the **Web of Science** (http://apps.webofknowledge.com), which **has data for 64** only publications.



Google scholar finds more references (880) in 77 works, but cannot separate self-citations, and calculates an h-index= 18. Removing the self citations we find **h-index= 17** (with **795 citations**).These citations are distributed to publications, in accordance to the following table. The second column represents the number of the publication (numbering as of section 12). In some publication, the citations of Scopus are more than of the Google Scholar, because of the different data sources they use. We could combine the two sources for more accurate results.

Similarly one can see most of my publications (73) listed at ORCID (ORCID ID: 0000-0002-7905-7530).

s/n	Article number (as of section 12)	Scholar citations	Scholar (without self-cit.)	Scopus citations
1	1	65	61	50
2	4	54	53	43
3	46	36	35	20
4	5	39	34	26
5	52	31	31	22
6	10	30	30	25
7	25	31	28	22
8	3	27	27	22
9	8	28	25	19
10	27	25	24	14
11	15	23	23	23
12	51	23	23	14
13	50	26	22	17
14	6	22	19	12
15	57	25	18	11
16	14	19	17	15
17	11	18	**17**	14
18	20	**18**	16	14
19	35	15	15	12

20	61	15	15	7
21	34	15	14	13
22	38	16	14	10
23	7	15	14	8
24	17	13	13	12
25	40	13	13	10
26	39	14	12	7
27	28	13	12	5
28	60	12	11	11
29	36	12	11	10
30	59	14	11	9
31	43	12	10	9
32	47	12	9	6
33	54	15	8	7
34	58	11	8	5
35	13	10	7	9
36	53	8	7	7
37	19	8	7	6
38	2	7	7	6
39	16	7	7	5
40	44	6	6	7
41	49	6	6	6
42	26	6	6	5
43	23	6	5	4
44	56	11	5	3
45	37	5	5	3
46	31	5	5	3
47	48	4	4	4
48	41	6	4	4
49	42	3	3	4
50	29	3	3	2
51	24	5	2	2
52	21	3	2	2
53	12	2	2	1
54	30	2	2	
55	9	2	1	2
56	22	1	1	1
57	18	1	1	1
58	S8	1	1	
59	S14	1	1	
60	32	2	1	
61	Σ1	1	1	
62	S7			1
63	S13	1		
	Total:	880	795	612