3rd WORKSHOP ON MODERN CIRCUITS AND SYSTEMS TECHNOLOGIES

March 14-15, 2014
Aristotle University Dissemination Center (ΚΕΔΕΑ)
Thessaloniki

PROGRAM - ABSTRACTS

AUTH e-LAB
Aristotle University of Thessaloniki-Electronics Laboratory

Organized by the FP7 Marie Curie IAPP Project FTK – Fast Tracker for Hadron Collider Experiments and Greek National Project NANOTRIM – Continuous Transistor Sizing Toolset for Nanoscale IC Optimization

PROGRAM

Friday, March 14

9:00	**Registration**
9:30	**Welcome Speech from Organizers and University Authorities:** ***Dr. S. Nikolaidis, Dr. K. Kordas*** – Department of Physics, AUTH, Greece ***Prof. S. Kouidou-Andreou*** – Vice Rector of Research, AUTH, Greece
9:45-10:45	**Plenary Talk:**
	Dr. Paola Giannetti – Director of Research, INFN Pisa Section, Italy *"High Performance Embedded Systems for High Energy Physics Experiments at Hadron Colliders"*
10:45-11:20	Coffee Break
Fast TracKer (FTK) IAPP Session	
11:20-11:40	***Dr. Francesco Crescioli*** – Researcher, LPNHE CNRS, France *"Associative Memories for Hadron Collider experiments: the FTK AMchip experience"*
11:40-12:00	***Daniel Magalotti*** – Researcher, INFN Perugia Section and University of Modena and Reggio Emilia, Italy *"The Associative Memory Board for the Fast TracKer (FTK) processor at ATLAS"*
12:00-12:20	***Calliope-Louisa Sotiropoulou*** – Researcher, Aristotle University of Thessaloniki, Greece *"A High Performance Parallel FPGA Implementation of a 2D-Clustering Algorithm for the ATLAS Fast TracKer (FTK) Processor"*
12:20-12:40	***Alessandro Iovene*** - Project Manager, CAEN SpA, Italy *"CAEN - Electronic Instrumentation for Nuclear Physics: R&D activities and innovative projects"*
12:40-13:00	***Petros Soukoulias*** – Head of the Scientific/Advisory Board and co-Founder, Prisma Electronics, Greece **"***Prisma Electronics – Electronics, Production Methods & Practices"*
13:00-14:15	Lunch Break
General Session	
14:15-14:40	***Dr. Nikos Bellas*** - Associate Professor, Department of Electrical and Computer Engineering, University of Thessaly, Greece *"Significance-Based Computing For Reliability and Power Optimization"*
14:40-15:00	***Panagiotis Mousouliotis*** – Novocaptis, Greece *"The EDUSAFE Project: System Architecture Challenges"*
15:00-15:20	***Dr. Yiorgos Tsiatouhas*** - Associate professor, Department of Computer Science and Engineering, University of Ioannina, Greece *"REliability Improvement of integrated circuits and systems in Nanometer technology (REIN): Recent research activity at the UoI"*
15:20-15:40	***Dr. Stavros Stavrinidis*** - Aristotle University of Thessaloniki, Greece *"Digital Chaos"*
15:40-16:00	***Dr. Giorgos Sirakoulis*** - Associate professor, Department of Electrical and Computer Engineering, Democritus University of Thrace, Greece *"Memristor: The Fourth fundamental electrical element"*
16:00:16:20	***Dr. Valantis Kavousianos*** - Assistant professor, Department of Computer Science and Engineering, University of Ioannina, Greece *"Testing for SoCs with Advanced Static and Dynamic Power-Management Capabilities"*

Saturday, March 15

9:45-10:45	**Plenary Talk:**
	Dr. Sotiris Bantas – CTO and co-founder, Helic Inc., Greece *"Building Chips for Better Apps: Silicon Design Technology Trends for Mobile and the Cloud"*
10:45-11:20	Coffee Break:
NANOTRIM Session	
11:20-11:40	***Prof. George Stamoulis***- Professor, Department of Electrical and Computer Engineering, University of Thessaly, Greece *"NANOTRIM: An overview"*
11:40-12:00	***Dr. Michalis Tsiampas*** - Helic Inc., Greece *"From research to product"*
12:00-12:20	***Charalampos Antoniadis*** - PhD candidate, Department of Electrical and Computer Engineering, University of Thessaly, Greece *"NanoTrim: A continuous transistor sizing tool"*
12:20-12:40	***Nikolaos Fasarakis*** - PhD candidate, Aristotle University of Thessaloniki, Greece *"An ultra-compact piecewise temperature depended analytical model for nanoscale bulk MOSFETs"*
12:40-13:00	***Panagiotis Chaourani*** - Msc. Aristotle University of Thessaloniki , Greece *"A Unified CMOS Inverter Model for Planar and FinFET Nanoscale Technologies"*
End of Workshop	

Workshop Organizing Committee	
	**Dr. Spyridon Nikolaidis, Associate Professor, Electronics Lab, Department of Physics, Aristotle University of Thessaloniki, Greece**
	**Dr. Kostas Kordas, Assistant Professor, Division of Nuclear and Elementary Particle Physics, Department of Physics, Aristotle University of Thessaloniki, Greece**
	**Calliope-Louisa Sotiropoulou, Researcher/PhD Candidate, Electronics Lab, Department of Physics, Aristotle University of Thessaloniki, Greece**

ABSTRACTS

PLENARY TALK - Friday, March 14

Dr. Paola Giannetti – Director of Research, INFN Pisa Sectio, Italy

Paola Giannetti is Research Director of INFN, Department of Pisa since 2002. She worked since 1982 at Hadron collider experiments, at Fermilab (Chicago) until 2009 and at CERN since that time, participating to the top quark and Higgs boson discoveries. She was proponent of the FTK processor for LHC experiments and was project leader of the INFN funded FTK R&D project (1999-2001). In addition, she was proponent of three trigger upgrades at CDF (Fermilab 2002-2008) and was responsible for INFN funds. Paola was FTK deputy project leader at ATLAS and responsible of INFN funds (2008-2012). She acted as Chair of the CMS experiment referee group in Italy (2007 and 2009), was scientist in charge of the FP6 OIF Marie Curie fellow POT and leader of the research program of FP7 IOF Marie Curie fellows ITES, ARTLHCFE and of the FP7 IAPP FTK program.

"High Performance Embedded Systems for High Energy Physics Experiments at Hadron Colliders"

Modern experiments search for extremely rare processes hidden in much larger background levels. Hadron colliders data flow is so massive that only a very small fraction of the produced collisions can be stored to tape. A drastic real-time data reduction must be obtained.

A multi-level trigger is an effective solution for an otherwise impossible problem. The level-1 trigger is based on custom processors and reduces the rate of a large factor in few microseconds. For higher level trigger selections large farms of commercial CPUs are usually preferred today, but there are important exceptions where powerful highly parallelized dedicated hardware provides excellent performances, much shorter latencies, saving energy (minor consumption), and space (much more compact systems).

I will report about my experience working with high-performance, highly parallelized hardware for the CDF experiment at the Fermilab Tevatron (Chicago, USA) and after that at the Atlas experiment at the Large Hadron Collider of CERN (Geneva, Switzerland), using a combination of technologies: powerful Field Programmable Gate Arrays (FPGAs) cooperating with standard-cell Application-Specific Integrated Circuits (ASICs) for utmost gate integration density.

Optimal partitioning of complex algorithms on a variety of computing technologies demonstrated to be a very powerful strategy.

PLENARY TALK - Saturday, March 15

Dr. Sotiris Bantas – CTO and co-founder, Helic Inc., Greece

Sotiris Bantas is CTO and co-founder of Helic, Inc.. He leads technology development since 2000 and is involved in the company's business development activities. Sotiris was awarded a degree in Electrical Engineering in 1995 and a Ph.D. in microelectronics in 2004, both from the National Technical University of Athens. Prior to Helic, he was a Research Engineer at the NTUA, and was involved in the design of silicon RF circuits, analog filters and data converters. Sotiris holds two US patents and has several pending. He also has some well-cited publications in peer-reviewed journals and conferences. He likes to work in the area of SoC design automation.

"Building Chips for Better Apps: Silicon Design Technology Trends for Mobile and the Cloud"

The advent of cloud computing has shifted the paradigm for the deployment and utilization of computer resources. It has also drastically altered the way internet-enabled businesses are being set up to deliver services to their customers. Data centers are constantly evolving to host the myriads of apps that are launching every day and causing vast amounts of data to move around the mobile infrastructure. To support this unprecedented technology growth, silicon ICs for mobile devices and data centers must evolve and provide more functionality and higher data rates, while complying with tight power and cost constraints. This talk focuses on selected areas of design technology, discussing how the various challenges are being addressed with advances in EDA tools and the silicon ecosystem as a whole. Clock frequencies are picking up again after years of relative stagnation, while serial data channels are currently pushing to 56 Gbps rates; some of this is fueled by transistor performance scaling, but retooling is also needed to rein in effects such as noise, crosstalk, power consumption and process variability.

Fast TracKer (FTK) IAPP Session

Dr. Francesco Crescioli – Researcher, LPNHE CNRS, France

"Associative Memories for Hadron Collider experiments: the FTK AMchip experience"

The AMchip is a VLSI device that implements the Associative Memory function, a special content addressable memory specifically designed for high energy physics applications and first used in the CDF experiment at Tevatron. Several generations of Associative Memory chips have been developed over the years.
The latest generation of AMchip has been developed for the core pattern recognition stage of the Fast TracKer (FTK) processor: a hardware processor for online reconstruction of particle trajectories at the ATLAS experiment at LHC. The algorithm for track finding using AMchips will be explained and the latest advancement in AMchip technology will be presented.

Daniel **Magalotti - Researcher, INFN Perugia Section and University of Modena and Reggio Emilia, Italy**

"The Associative Memory Board for the Fast TracKer (FTK) processor at ATLAS"

The Associative Memory (AM) system of the FTK processor has been designed to perform pattern matching using the hit information of the ATLAS silicon tracker. The AM is the heart of the FTK processor and it finds track candidates at low resolution that are seeds for a full resolution track fitting.
The Associative Memory System consists of the AM chip, an ASIC designed to perform pattern matching, and two types of boards, the Local Associative Memory Board (LAMB), a mezzanine where the AM chips are mounted, and the Associative Memory Board (AMB).
In this talk, we describe the evolution of the AM boards, starting from a "Parallel Rrocessor", based on parallel connections to a "Serial Link Processor", based on a network of 2 Gb/s serial links. We report also on the performance of first prototypes and the tests of the integrated system.

Calliope-Louisa Sotiropoulou – Researcher, Aristotle University of Thessaloniki, Greece

"A High Performance Parallel FPGA Implementation of a 2D-Clustering Algorithm for the ATLAS Fast TracKer (FTK) Processor"

The high performance parallel 2D-clustering FPGA implementation used for the input system of the ATLAS Fast TracKer (FTK) processor is presented. The input system for the FTK processor will receive data from the Pixel and micro-strip detectors read out drivers (RODs) at 760Gbps, the full rate of level 1 triggers. Clustering serves two purposes. The first is to reduce the high rate of the received data before further processing. The second is to determine the cluster centroid to obtain the best spatial measurement. For the pixel detectors the clustering is implemented by using a 2D-clustering algorithm that takes advantage of a moving window technique to minimize the logic required for cluster identification. The implementation is fully generic,

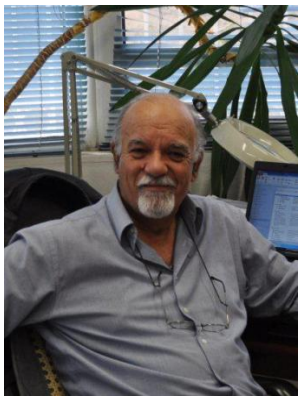
therefore the detection window size can be optimized for the cluster identification process. Additionally, the implementation can be parallelized by instantiating multiple cores to identify different clusters independently. This flexibility makes the implementation suitable for a variety of demanding image processing applications. The implementation is robust against bit errors in the input data stream, drops all data that cannot be identified, but also reintroduces missing control words when necessary. The parallel 2D-clustering implementation has sufficient processing power to meet the specification for the Pixel layers of ATLAS, for up to 80 overlapping pp (proton-proton) collisions that correspond to the maximum LHC luminosity planned until 2022.

Alessandro Iovene - Project Manager, CAEN SpA, Italy

"CAEN - Electronic Instrumentation for Nuclear Physics: R&D activities and innovative projects"

CAEN is recognized as one of the most important industrial players in the Nuclear Physics research market. CAEN is also involved in several leading-edge R&D collaborative projects, each of them with these common goals: to continue to expand and develop its expertise in high-level electronic design, and to extend this expertise into complementary and relevant applications for the benefit of the community as a whole. A particular focus of these R&D collaborative projects has been in the fields of SECURITY (CBRNE Protection, Illicit Trafficking Countermeasures, Radiation Monitoring of Sensitive Locations, etc...) and the ENVIRONMENT (Environmental Radioactivity Monitoring, Recognition of Radioactive Contamination Threats, etc...).players in the Nuclear Physics research market. Since its establishment in 1979, CAEN operates in a highly specialized international market: the design, the production and the supply of electronic instrumentation for radiation and low light sensors. CAEN products are used in the most prestigious laboratories, universities and research centers of the world. The company operative field is focused on two main areas: nuclear physic research (both high and medium-low energies) and its fall-out applications.

Petros Soukoulias – Head of the Scientific/Advisory Board amd co-Founder, Prisma Electronics, Greece



Petros Soukoulias is the Head of the Scientific/Advisory Board and co-Founder of Prisma Electronics SA. He established the electronics sector of the Company, under his capacity of the General Manager (1997-2010). Since 2005, he is the project coordinator in all CERN, ESA and other European large-scale projects, leading Prisma Electronics to the CMS industry gold award in 2009. At the present time, he coordinates the FP7 ITN EDUSAFE and FP7 IAPP FTK programs.

Petros Soukoulias is the Head of the Regional Council for Innovation & Entrepreneurship in Eastern Macedonia and Thrace.

"Prisma Electronics – Electronics, Production Methods & Practices"

The production of Electronics is a complicated and delicate process. Personnel experience and proper equipment are fundamental factors for a high quality result. The methods and practices followed evolve on a daily basis, targeting precision, speed and above all quality.

Production materials also follow the evolution with improved tolerance and longer operational time. These are the prerequisites of a modern electronics production environment to carry out simple up to very advanced applications.
Although speed and capacity are the main objectives for the designers, miniaturization is the the challenge for the manufacturers. So, the trend, we have to support, is :
'Higher functionality (faster processing & larger memory) in lower volume Electronic devices.'

General Session

Dr. Nikos Bellas - Associate Professor, Department of Electrical and Computer Engineering, University of Thessaly, Greece

"Significance-Based Computing For Reliability and Power Optimization"

Manufacturing process variability at low geometries and energy dissipation are the most challenging problems in the design of future computing systems. Currently, manufacturers go to great lengths to guarantee fault-free operation of their products by introducing redundancy in voltage margins, conservative layout rules, and extra protection circuitry.
However, such design redundancy leading to significant energy overheads may not be really required, given that many modern workloads, such as multimedia, machine learning, visualization, etc. can tolerate a degree of imprecision in computations and data.
In this talk, I will introduce SCoRPiO, an approach which seeks to exploit this observation and to relax reliability requirements for the hardware layer by allowing a controlled degree of imprecision to be introduced to computations and data. It proposes to research methods that allow the system- and application-software layers to synergistically characterize the significance of various parts of the program for the quality of the end result, and their tolerance to faults. Based on this information, extracted automatically or manually, the system software will steer computations and data to either low-power, yet unreliable or higher-power and reliable functional and storage components. In addition, the system will be able to aggressively reduce its power footprint by opportunistically powering hardware modules below nominal values.
Significance-based computing lays the foundations for not only approaching the theoretical limits of energy reduction of CMOS technology, but also moving beyond those limits by accepting hardware faults in a controlled manner. Reliability issues in SCoRPiO are not seen as a problem but rather as an opportunity to rethink the concept of computation in a novel way that will allow semiconductor industry to progress beyond 22nm nodes. The ideas developed in this proposal are going to be valid irrespective of the technology and the materials and may help alleviate any reliability and energy issues in the beyond-Moore era.

Panagiotis Mousouliotis – Novocaptis, Greece

"The EDUSAFE Project: System Architecture Challenges"

EDUSAFE is a 4-year Marie Curie ITN project, which focuses on research into advanced Virtual Reality (VR) and Augmented Reality (AR) technologies for a personnel safety system platform. The aim of this safety system platform is to be used during planned and emergency maintenance in extreme environments (nuclear installations, space, deep sea, etc.).

The result of the EDUSAFE project will be a prototype which will include an integrated wearable VR/AR system and a control system. The system architecture challenges of this prototype include the design of the performance/power/size-constrained wearable system, the real-time wireless data transmission to/from the control system, and the instantaneous analysis of the data coming from different inputs (e.g. the personnel wearable systems, various sensors installed in the work environment) at the control system.

Dr. Yiorgos Tsiatouhas - Associate professor, Department of Electrical and Computer Engineering, University of Ioannina, Greece

"REliability Improvement of integrated circuits and systems in Nanometer technology (REIN): Recent research activity at the UoI"

Integrated circuit reliability is a major concern in the nanometer era. The REIN project aims on the development of innovative solutions that will maintain increased reliability in nanometer technology integrated circuits and systems. In this lecture, we will present resent research activities at the VLSI Technology and Computer Architecture Lab of the University of Ioannina (UoI) under the REIN project. Resilient circuit design techniques that provide error tolerance during the circuit operation in the field will be discussed. In addition, the concept of reusing the existing testing circuitry in both off-line (or periodic) and concurrent testing procedures will be accentuated.

Dr. Stavros Stavrinidis - Aristotle University of Thessaloniki, Greece
"Digital Chaos"

"Digital Chaos"

Chaos is a universal phenomenon, exhibited by complex systems. Although it seems to be random, it is not stochastic, but deterministic. Since nonlinear circuit behavior has attracted the interest of the scientific and engineering community, during the last decades, numerous circuits have been presented. Next to that, experimental study and verification of chaotic phenomena, utilizing nonlinear circuits, have been portrayed. Moreover, applications of chaotic operating nonlinear circuits have appeared, mainly in the area of secure communications or ultra-wideband data transmission. In all cases the circuits employed, were analog ones; very rarely mixed signal circuits have been proposed.

On the other hand, digital, chaotic-operating circuits have not been on the mainstream of circuit design, till today. A digital circuit exhibiting chaotic behavior would combine all benefits that digital technology embosoms, i.e. easy circuit applicability, matching free and easy upgrade to fabrication process improvements, together with inherent advantages that nonlinear circuits demonstrate. Depending on the applications that are supposed to be used, digital chaotic circuits could be utilized as random number generators, oscillators, or synchronized chaotic transmitters – receivers.

In this talk a communication system based on chaotic synchronization, suitable for secure and UWB transmission in introduced. The transmitter is an all-digital chaotic operating electronic circuit, suitable for information modulation and secure chaotic transmission. The chaotic oscillating circuit is a non-autonomous one and it is designed in such a way that

signals at all stages are digital ones. In this case, the nonlinearity demanded is realized by means of digital design. No analog sub-circuit is involved in generating chaos. Oscillator design and demonstration of its chaotic behavior is provided, together with the evaluation of the chaotic properties that it possesses, employing established nonlinear dynamics tools. The receiver is an almost identical circuit synchronized to transmitter, being capable of extracting the information modulated by the transmitter. An early evaluation of the overall system will be also presented.

Dr. Giorgos Sirakoulis - Associate professor, Department of Electrical and Computer Engineering, Democritus University of Thrace, Greece

"Memristor: The Fourth fundamental electrical element"

Over 30 years ago Leon Chua proposed the existence of a new class of passive circuit elements, which he called memristors and memristive devices. Since then emerging chip technologies utilizing novel devices and materials are continuously becoming attractive alternatives to conventional CMOS technology, which is challenged by its technological physical limits. The identification of Chua's memristor in 2008 by HP Labs originated intense research activity in the field. The unique electrical characteristics associated with them, along with the advantages of crossbar structures, have the potential to revolutionize computing architectures. Recently, many researchers have worked actively on multiple applications of memristors ranging from memory and reconfigurable logic, to neuromorphic engineering, generating new opportunities for analog and digital circuits. This presentation aims to address a novel research area taking into account memristor characteristics and properties and motivate for further research on new design strategies that comply with emerging technologies and with the oncoming scale-down of the electronic circuits.

Dr. Valantis Kavousianos - Assistant professor, Department of Electrical and Computer Engineering, University of Ioannina, Greece

"Testing for SoCs with Advanced Static and Dynamic Power-Management Capabilities"

Many multicore chips today employ advanced power management techniques. Multi-threshold CMOS (MTCMOS) is very effective for reducing standby leakage power. Dynamic voltage scaling and voltage islands which operate at multiple power-supply voltage levels, minimize dynamic power consumption. Effective defect screening for such chips requires advanced test techniques that target defects in the embedded cores and the power management structures. We describe recent advances in test generation and test scheduling techniques for SoCs that support power switches, voltage islands, and dynamic voltage scaling schemes.

NANOTRIM Session

Prof. George Stamoulis - Professor, Department of Electrical and Computer Engineering, University of Thessaly, Greece

"NANOTRIM: An overview"

The NANOTRIM project (Continuous Transistor Sizing Toolset for nanoscale IC optimization) aims to make significant advances in Electronic Design Automation (EDA) technology, to develop key enablers for the performance optimization of nanoscale integrated circuits (ICs) and allow for significantly more power-efficient chips. This is targeted by means of innovative methods and algorithms for physical (i.e. gate- and transistor-level) synthesis, which are pioneered by the partners. Optimal continuous transistor/device sizing has been a holy grail in the EDA community. However, efforts to this end have been hampered by the sheer size of the optimization problem (millions of variables and constraints), modeling issues –especially in the timing domain– as well as the problem of generating a DRC clean (i.e. manufacturable) layout that implements the calculated optimal transistor sizes. The proposed activity is building on the learnings from both academic and industrial attempts to tackle a difficult yet attractive design problem. The approach taken is to perform continuous sizing optimization but in a constrained mode, in order to arrive at solutions that are reliably implemented in silicon, and easily integrated into mainstream design flows. Our team brings together experience in all areas required to not only provide a world-class solution to the continuous sizing problem but also to eventually, successfully incorporate this solution into a viable product, addressing all issues that have prevented previous academic and industrial efforts from arriving at this goal.

Dr. Michalis Tsiampas - Helic Inc., Greece

"From research to product"

This presentation will discuss Nanotrim's market driven approach and exploitation awareness, as well as how the cooperation between academic and industrial partners can lead to industrial prototype with market potential.

Charalampos Antoniadis - PhD candidate, Department of Electrical and Computer Engineering, University of Thessaly, Greece

"NanoTrim: A continuous transistor sizing tool"

Optimal continuous transistor/device sizing has been a holy grail in the EDA community. However, efforts to this end have been hampered by the sheer size of the optimization problem (millions of variables and constraints), modeling issues – especially in the timing domain– as well as the problem of generating a DRC-clean (i.e. manufacturable) layout that implements the calculated optimal transistor sizes. This research work proposes NanoTrim, a continuous transistor sizing tool taking into consideration power and timing constraints, in order to arrive at solutions that are reliably implemented in silicon, and easily

integrated into mainstream design flows. NanoTrim comprises a hybrid heuristic approach and state-of-the-art algorithms for finding the optimal transistor sizes and resizing the layout in a DRC-clean fashion. In addition, NanoTrim can exploit the computational power of parallel architectures in order to decrease execution time and enable analysis of very large-scale integrated circuits.

Nikolaos Fasarakis - PhD candidate, Aristotle University of Thessaloniki, Greece

"An ultra-compact piecewise temperature depended analytical model for nanoscale bulk MOSFETs"

An accurate ultra-compact model for nanometer CMOS transistors, suitable for digital circuit simulations relative to static and transient circuit analysis problems, is proposed. Six physical-like fitting parameters are used to achieve high accuracy. The model is applied separately for every region of operation and the parameters are extracted through trivial optimization techniques. Here, the model is verified through simulation results (PTM) in 45-nm CMOS technology in terms of the channel width (from 45nm to 900nm) and the temperature (from 0^{o}C to 120^{o}C) for both n- and p-type bulk MOSFETs.

Panagiotis Chaourani - Msc. Aristotle University of Thessaloniki, Greece

"A Unified CMOS Inverter Model for Planar and FinFET Nanoscale Technologies"

In this paper, a new analytical model for describing the output waveform of the CMOS inverter for planar and FinFET nanoscale technologies, is introduced. A modified expression for the transistor current is adopted taken into account nano-scale effects like DIBL, CLM and NWE. The sub-threshold current of both transistors as well as their drain-to-bulk capacitances, which influence significantly the accuracy, are also considered. The proposed model has been validated through comparisons with HSPICE simulations for a wide range of different circuit configurations (supply voltage, output load, slew rate, transistor sizes, temperature). The comparisons concerned the propagation delay accuracy as well as the CPU time of the calculations.